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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,527	11/01/2001	Fabrice Marinet	00RO27154259	4394

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ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
CERVETTI, DAVID GARCIA	
ART UNIT	**PAPER NUMBER**
2136	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,527	MARINET ET AL.	
	Examiner	Art Unit	
	David G. Cervetti	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 16-45 are pending and have been examined.

2. Applicant's arguments filed June 1, 2005, have been fully considered.

Response to Amendment

3. Examiner approves the amendment to the specification. The objection to the specification is withdrawn.

4. The objection to the drawings is withdrawn.

5. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

6. Examiner submits that the use of timers to determine disabling devices was well known in the art.

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 16-17, 22-24, 29-33, 37-41, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yach et al. (US Patent Number: 5,454,114 hereinafter "Yach"), and further in view of Green (US Patent Number: 4,769,765).

Regarding claim 16, Yach teaches detecting the state of at least one timer before a predetermined processing sequence performed by the integrated circuit; if the at least one timer is not activated, performing the processing sequence and activating

the at least one timer; and disabling the integrated circuit and preventing the processing sequence from being performed (column 12, lines 42-67, column 13, lines 1-67). Yach does not expressly disclose disabling the integrated circuit if the at least one timer is activated. However, Green teaches using timers to disable a device (column 3, lines 8-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Green with the integrated circuit of Yach. One of ordinary skill in the art would have been motivated to perform do so because it was well known in the art to protect circuits from tampering (Green, column 3, lines 33-67).

Regarding claim 23, Yach teaches providing at least one timer associated with the CPU (figure 5); detecting a state of the at least one timer before beginning an operating session of the integrated circuit; activating the at least one timer if it is not activated and beginning the operating session; and disabling the integrated circuit (column 12, lines 42-67, column 13, lines 1-67). Yach does not expressly disclose disabling the integrated circuit if the at least one timer is activated. However, Green teaches using timers to disable a device (column 3, lines 8-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Green with the integrated circuit of Yach. One of ordinary skill in the art would have been motivated to perform do so because it was well known in the art to protect circuits from tampering (Green, column 3, lines 33-67).

Regarding claim 30, Yach teaches at least one timer circuit comprising a timer designed to remain in an activated state as long as the circuit is powered-on and for a

predetermined duration if the circuit is powered-off, means for activating the timer, means for deactivating the timer, and means for detecting the activated or deactivated state of the timer; and means for reading the timer state and for disabling the integrated circuit at predefined times (column 12, lines 42-67, column 13, lines 1-67). Yach does not expressly disclose disabling the integrated circuit if the at least one timer is activated. However, Green teaches using timers to disable a device (column 3, lines 8-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Green with the integrated circuit of Yach. One of ordinary skill in the art would have been motivated to perform do so because it was well known in the art to protect circuits from tampering (Green, column 3, lines 33-67).

Regarding claim 38, Yach teaches a central processing unit (CPU) (figure 5); at least one timer circuit and comprising a timer which is activated when the IC is powered-on and for a predetermined duration when the IC is powered-off, a timer activating circuit for activating the timer, a timer deactivating circuit for deactivating the timer, and a detection circuit for detecting the state of the timer; and an IC disabling circuit for disabling the IC at predefined times (column 12, lines 42-67, column 13, lines 1-67). Yach does not expressly disclose disabling the integrated circuit if the at least one timer is activated. However, Green teaches using timers to disable a device (column 3, lines 8-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Green with the integrated circuit of Yach. One of ordinary skill in the art would have been

motivated to perform do so because it was well known in the art to protect circuits from tampering (Green, column 3, lines 33-67).

Regarding claims 17 and 24, the combination of Yach and Green teaches the limitations as set forth under claims 16 and 23 respectively above. Furthermore, Yach teaches resetting a timer based on a predetermined condition (column 13, lines 1-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to deactivate a timer if a condition is met. One of ordinary skill in the art would have been motivated to do so because it was well known in the art at the time the invention was made to take predetermined actions based on the status of a timer.

Regarding claims 22 and 29, the combination of Yach and Green teaches the limitations as set forth under claims 16 and 23 respectively above. Furthermore, Yach teaches wherein the at least one timer comprises a plurality of timers each being associated with a respective authentication calculation of a sequence of a predefined number of calculations; and further comprising: detecting the state of a respective timer before performing an associated calculation, activating the respective timer if it is not activated, and disabling the integrated circuit if the respective timer is activated (column 12, lines 42-67, column 13, lines 1-67).

Regarding claims 31 and 39, the combination of Yach and Green teaches the limitations as set forth under claims 30 and 38 respectively above. Furthermore, Yach teaches resetting a timer based on a predetermined condition (column 13, lines 1-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to deactivate a timer after normal execution of a predetermined processing sequence. One of ordinary skill in the art would have been motivated to do so because it was well known in the art at the time the invention was made to take predetermined actions based on the status of a timer.

Regarding claims 32 and 40, the combination of Yach and Green teaches the limitations as set forth under claims 30 and 38 respectively above. Furthermore, Yach teaches wherein each timer circuit further comprises: detecting a power supply (column 12, lines 29-67); and allowing the timer to be activated or deactivated when the power supply is detected during a predetermined time period (column 13, lines 1-67).

Regarding claims 33, the combination of Yach and Green teaches the limitations as set forth under claim 30 above. Furthermore, Yach teaches wherein the at least one timer circuit comprises a plurality of timer circuits, each timer circuit being associated with an authentication calculation performed by the integrated circuit; and further comprising means for determining, before each calculation, the state of the timer associated with the calculation, activating the associated timer if it is not activated and disabling the integrated circuit if the associated timer is activated (column 12, lines 42-67, column 13, lines 1-67).

Regarding claims 37 and 45, the combination of Yach and Green teaches the limitations as set forth under claims 30 and 38 respectively above. Furthermore, Yach teaches a test circuit for reducing the predetermined duration of the timer during a testing procedure (column 19, lines 10-67).

Regarding claims 41, the combination of Yach and Green teaches the limitations as set forth under claim 38 above. Furthermore, Yach teaches wherein the at least one timer circuit comprises a plurality of timer circuits each being associated with an authentication calculation performed by the IC (column 12, lines 42-67, column 13, lines 1-67).

9. Claims 18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yach and Green, and further in view of Schrenk (US Patent Number: 5,497,462).

Regarding claims 18 and 25, the combination of Yach and Green does not expressly disclose modifying the value of a counter, comparing a value to a threshold value, or performing an action based on the threshold. However, Schrenk teaches modifying the value of a counter within a protected area in a non-volatile memory if it is detected that the at least one timer is activated (column 5, lines 1-7); comparing the counted value with a predefined threshold (column 5, lines 12-15); and performing a process for protecting confidential data stored within memories in the integrated circuit if the counted value reaches the predefined threshold (column 2, lines 52-55). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a counter in a non-volatile memory and to compare the value of the counter to a threshold value. One of ordinary skill in the art would have been motivated to perform such a modification to prevent circumventing the limitation of the number of attempts (Schrenk, column 2, lines 28-41).

10. Claims 19-21 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yach, Green, and Schrenk, and further in view of Sutherland (US Patent Number: 6,292,898).

Regarding claims 19 and 26, the combination of Yach, Green, and Schrenk does not expressly disclose wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

Regarding claims 20 and 27, the combination of Yach, Green, and Schrenk does not expressly disclose wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

Regarding claims 21 and 28, the combination of Yach, Green, and Schrenk does not expressly disclose wherein the protection process comprises erasing all memories in the integrated circuit. However, Sutherland teaches wherein the protection process comprises erasing all memories in the integrated circuit (column 1, lines 43-50, column 4, lines 34-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to erase data upon tamper detection. One of ordinary skill in the art would have been motivated to perform such a modification to prevent the tamperer from preserving the stored data (Sutherland, column 4, lines 27-35).

11. Claims 34-36 and 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yach and Green, and further in view of Brehmer et al. (US Patent Number: 5,563,799, hereinafter "Brehmer").

Regarding claims 34 and 42, the combination of Yach and Green does not expressly disclose a timer circuit comprises: a capacitor; a discharge circuit associated with the capacitor and designed so that the capacitor slowly discharges when the device is powered-off; a circuit for detecting capacitor charging; means for controlling capacitor charging; and means for controlling capacitor discharging. However, Brehmer teaches wherein the at least one timer circuit comprises: a capacitor (column 3, lines 65-66); a discharge circuit associated with the capacitor and designed so that the capacitor slowly discharges when the device is powered-off (column 4, lines 41-47); a circuit for detecting capacitor charging (column 4, lines 41-47); means for controlling capacitor charging (column 4, lines 41-47); and means for controlling capacitor discharging

(column 4, lines 41-47). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a capacitor with the timer circuit to operate in response to current flowing through the circuit. One of ordinary skill in the art would have been motivated to perform such a modification to help detect a malfunction condition (Brehmer, column 4, lines 10-15).

Regarding claims 35 and 43, the combination of Yach, Green, and Brehmer teaches the limitations as set forth under claims 34 and 42 respectively above. Furthermore, Brehmer teaches wherein the means for controlling capacitor discharging is designed for discharging the capacitor more rapidly than when the device is powered-off (column 5, lines 25-42).

Regarding claims 36 and 44, the combination of Yach, Green, and Brehmer teaches the limitations as set forth under claims 34 and 42 respectively above. Furthermore, Brehmer teaches wherein the at least one timer circuit further comprises a MOS transistor associated with the capacitor so that it is only discharged by a leakage current when the integrated circuit is powered-off (column 3, lines 55-57, column 6, lines 62-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571) 272-5861. The examiner can normally be reached on Monday-Friday 7:00 am - 5:00 pm, off on Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DGC

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100